REMARKS

Claims 11-21 are pending in the application. The status of the claims is as follows:

Claims	Status
14, 19	Allowed/allowable
11-13, 15-18, and 20-21	Rejected

The rejected claims / sections were rejected as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
Drawings	Objection	• Every feature not shown
11	Objection	• Lacking clarifying verbage
11-13, 15-18, & 20-21	§102(e) Anticipation	• Uehara, et al. (U.S. Patent No. 5,698,902) .

Applicants have amended claim 11 and provided discussion distinguishing the Uehara disclosure from the present invention. Applicants thank the Examiner for indicating the allowability of claims 14 and 19.

Applicants respectfully note that in the explanations provided below, the use of reference characters is for providing clarification for an exemplary embodiment and should not be construed as limiting the invention in any manner beyond the broadest reasonable interpretation without reference characters.

Missing Initialed PTO-1449 Form

1. Applicants note that an initialed PTO-1449 form indicating consideration of the references in the IDS submitted with the Preliminary Amendment on January 14, 2000 has not been received in the case.

Applicants are providing a copy (Appendix C) of the PTO-1449 form submitted with the Preliminary Amendment in this case, and respectfully request that an initialed form be returned with the next communication from the U.S. Patent

Office.

Priority

2. Applicants are submitting the cover sheet of the German priority document as Appendix D and ask that the Examiner obtain a copy of the priority document from the International Bureau.

Applicants are submitting the cover sheet of the German priority document. The German parent application 19730974.7 was dropped and the file was destroyed by the German Patent and Trademark Office—the priority document remaining at this office only consists of the cover sheet.

Applicants note that the loss of the priority document appears to be the fault of the U.S. Patent Office, as the Notification of Acceptance of Application under 35 U.S.C 371 and 37 C.F.R 1.494 and 1.495, mailed March 7, 2000 (enclosed in Appendix B), clearly indicates that the priority document was received by the U.S. Patent Office from the International Bureau. Applicants are, as a courtesy, attempting to obtain a copy from the International Bureau, but respectfully assert that the claim of foreign priority should be accepted by the U.S. Patent Office.

Drawings

3. Applicants believe that the drawings sufficiently show "said conductive filler structure being conductively connected to said doped region" when considered in the context of the detailed description of the invention.

Applicants believe that the drawings show "said conductive filler structure being conductively connected to said doped region" as described below.

The Examiner indicated on p. 2, sec. 2 of the OA that the conductive filler structure 72 cannot be conductively connected to the doped region 3 because the conductive filler structure 72, according to Figs. 3-7, is placed on the insulation

trenches 2, and these trenches prevent conductivity between the conductive filler structure 72 and doped region 3.

However, as exemplified in Fig. 6 and using an exemplary embodiment with reference characters, the conductive filler structure 72 *is* conductively connected with the doped region 3 via the overlapping contact 132, which is made of, e.g., tungsten, and the well contact 10.

The Specification states, at 7/7-13:

> By filling the via holes with metal, for example tungsten, contacts 131 to the source/drain region 9 and the conductive useful structure 71 and an overlapping contact 132 to the well contact 10 and the neighboring, conductive filler structures 72 are formed (see Figure 6). The overlapping contact 132 is in communication both with the surface of the neighboring, conductive filler structures 72 as well as with the surface of the well contact. As a result thereof, the filler structures are connected to the doped well 3 via the well contact 10.

The well contact 10 being conductive is inferred in the Specification by its use and by its composition as disclosed at 6/24-25.

> The well contact 10 is doped, for example, with boron and comprises a dopant concentration of 6×10^{19} at/cm^3.

This concentration renders the well contact 10 conductive.

For these reasons, Applicants contend that "said conductive filler structure being conductively connected to said doped region" is adequately disclosed by the drawings and the related description, and respectfully request that the objection to the drawings be withdrawn from the application.

Claim Objections

4. Applicants have amended claim 11 to include the word "semiconductor" before "substrate".

In accordance with the suggestion of the Examiner, Applicants have

amended claim 11 so that the pertinent portion reads "said semiconductor substrate". Applicants respectfully request withdrawal of this rejection from the application.

35 U.S.C. §102(e), Claims 11-21 Anticipation by Uehara '902

5. Uehara does not teach or suggest a conductive filler structure that is conductively connected to a doped region.

The independent claims of the present invention contain a limitation that the conductive filler structure (72) is *conductively connected* to the doped region (3).

As Applicants argued in the last response (with respect to Uehara's Fig. 6, but Figs. 7a to 9e refer to the same second embodiment as Fig. 6 does—see 9/7-19) that Uehara shows dummy electrodes being insulated from the doped regions, thereby teaching away from the present invention. Applicants reassert these arguments in the present response.

Uehara teaches (referring to Figs. 6 and 7a-9e) that the dummy electrodes 50b (and corresponding layers 16b and 18b) are *insulated from* the doped regions (source/drain regions 21, 21a, 21b) by insulating films (gate insulating film 15a and dummy insulating film 15b, and dummy protective film 19b).

The invention of the present application addresses problems with an integrated circuit arrangement having conductive structures used as gate electrodes and with conductive filler structures used as dummy structures. In these circuits, the dummy structures do not have any electrical function in the integrated circuit arrangement but they are required for improving planarity when manufacturing the integrated circuit arrangement. The dummy structures are provided in those regions of the semiconductor substrate surface where the geometrical density of conductive structures is very low.

These integrated circuits, however, have a problem in that the electrically conductive filler structures become charged. According to the present invention this problem is solved by connecting these filler structures with conductive doped region in the semiconductor substrate material, possibly with the aid of an electric contact. One possible contact is illustrated in Figure 7 of the present application (see reference No. 132) and may have a T-shaped form. At the bottom of an exemplary T-shaped contact 132, the doped well 3 in the substrate 1 is contacted. At the bottom of the broadened upper portion of the contact 132 a dummy filler structure 72 is contacted. This eliminates the problematic charging of the filler structure.

In more detail, Uehara does not teach or suggest the present invention because there is no electrical contact between the dummy structure 50b (or its layers 16b, 18b) and a doped region.

Uehara shows withdrawn electrode metal layers 31 contacting doped regions 21, 21b which are source/drain regions of the MOSFET comprising the gate electrode 50a. The withdrawn electrode metal layers 31 serve to provide electric contacts 33, 34 of the source/drain regions at a larger distance from the gate electrode stack 50a. The metal layers 31 do not serve as electrical contacts between the dummy structures 50b and the doped source/drain regions 21, 21b since there is no conductive connection between the dummy structure 50b and the metal layer 31. The dummy structure 50b comprising the conductive layers 16b, 18b is surrounded by a dummy insulating film 15b underneath (see column 13, line 11), a protective insulating film l9b (see column 13, line 8), a dummy spacer 20b (see column 13, line 15) and an isolation region 17 (see column 13, lines 3 to 4). All of these layers and regions are made of silicon dioxide and therefore are isolating rather than conductive. In particular the protective insulating film 19b prevents an electric

contact between the dummy structure 50b and the withdrawn electrode metal layer 31. For detailed description of figure 6 see column 12, line 56 to column 13, line 58.

Thus, even though Uehara deals with dummy structures used for improved pattern dimensions, it teaches away from the present invention because it does not teach or suggest an electric contact between a dummy structure and a doped well in a substrate that could be used to carry away the problematic charges of the dummy structures.

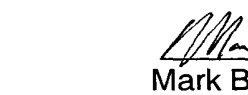
For these reasons, Applicants assert that the claim language clearly distinguishes over the prior art, and respectfully request that the Examiner withdraw the §102 rejection from the present application.

CONCLUSION

Inasmuch as each of the rejections have been overcome by the amendments and arguments presented, and all of the Examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be reconsidered, the rejections be withdrawn and that this application be passed to issue.

Applicants respectfully request that the finality of the last Office Action be withdrawn so that the Preliminary Amendment may be considered by the Examiner.

Respectfully submitted,

 (Reg. No. 45,877)

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on January 28, 2003.

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APPENDIX A
MARKED-UP CLAIMS

11. (Amended) An integrated circuit arrangement comprising:

a semiconductor substrate having at least one doped region; and

a plane arranged on a surface of said semiconductor substrate and having a number of conductive useful structures and at least one conductive filler structure, said conductive filler structure being conductively connected to said doped region.

APPENDIX B
COPY OF NOTIFICATION OF ACCEPTANCE

APPENDIX C
ORIGINALLY SUBMITTED PTO-1449 FORM

APPENDIX D
COVER SHEET OF PRIORITY DOCUMENT